AMENDMENTS

In the Claims:

Please amend claims 1, 6, 10, 18 and 22 as follows:

Claim 1 (Currently amended): A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated on a channel region which receives a first input signal, wherein the channel region is formed between said source region and drain region and a gate electrode receives the first input signal which influences the channel region through a gate insulating film, wherein:

each of said semiconductor elements is electrically separated from the others;

said well in each of said semiconductor elements is provided with a substrate terminal which receives a second input signal through a contact hole formed therein at a region other than said source region and drain region; and

the first and second input signals are different signals that are synchronized with each other.

Claim 2 (original): The semiconductor device of Claim 1, wherein operating characteristics are changed by adjusting impurity concentration in said channel region and levels of a high voltage and a low voltage applied to said gate terminal and substrate terminal.

Claim 3 (original): The semiconductor device of Claim 1, wherein said semiconductor layer in each of said semiconductor elements is electrically separated from each other by means of an oxide film.

Claims 4-5 (withdrawn)

Claim 6 (Currently amended): The semiconductor device of Claim 1, wherein:

each of said semiconductor elements is composed of ~~a pair of~~ a P-type semiconductor element and an N-type semiconductor element;

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

a gate terminals of said P-type semiconductor element is connected to a gate terminal of said ~~and~~ N-type semiconductor element ~~are connected to each other~~, thereby to form the first input terminal;

a substrate terminals of said P-type semiconductor element is connected to a substrate terminal of said ~~and~~ N-type semiconductor element ~~are connected to each other~~, thereby to form the second input terminal; and

a drain terminals of said P-type semiconductor element is connected to a drain terminal of said ~~and~~ N-type semiconductor element ~~are connected to each other~~, thereby to form an output terminal.

Claim 7 (withdrawn)

Claim 8 (original): The semiconductor device of Claim 6, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

Claim 9 (withdrawn)

Claim 10 (Currently amended): A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated on a channel region, formed between said source region and drain region, through a gate insulating film, wherein:

each of said semiconductor elements is electrically separated from the others;

said well in each of said semiconductor elements is provided with a substrate terminal through a contact hole formed therein at a region other than said source region and drain region;

[each of said semiconductor elements is composed of ~~a pair of~~ a P-type semiconductor element and an N-type semiconductor element;]

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form a first input terminal;

a gate terminal of said N-type semiconductor element and a substrate terminal of said P-type semiconductor element are connected to each other, thereby to form a second input terminal; and

a drain terminals of said P-type semiconductor element is connected to a drain terminal of said ~~and~~ N-type semiconductor element ~~are connected to each other~~, thereby to form an output terminal.

Claim 11 (withdrawn)

Claim 12 (original): The semiconductor device of Claim 10, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said first input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said high potential.

Claim 13 (withdrawn)

Claim 14 (original): The semiconductor device of Claim 6, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said low potential and lower than said high potential when said second input terminal is supplied with said low potential, and lower than said low potential when said second input terminal is supplied with said high potential.

Claim 15 (withdrawn)

Claim 16 (original): The semiconductor device of Claim 10, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said second input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said low potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said first input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said low potential.

Claim 17 (withdrawn)

Claim 18 (Currently amended): A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated on a channel region, formed between said source region and drain region, through a gate insulating film, wherein:

each of said semiconductor elements is electrically separated from the others;

said well in each of said semiconductor elements is provided with a substrate terminal through a contact hole formed therein at a region other than said source region and drain region;

[each of said semiconductor elements is composed of ~~a pair of~~ a P-type semiconductor element and an N-type semiconductor element;]

a drain terminal of said N-type semiconductor element is supplied with a high potential and a drain terminal of said P-type semiconductor element is supplied with a low potential;

a gate terminals of said P-type semiconductor element is connected to a gate terminal of said ~~and~~ N-type semiconductor element ~~are connected to each other~~, thereby to form a first input terminal;

a substrate terminals of said P-type semiconductor element is connected to a substrate terminal of said ~~and~~ N-type semiconductor element ~~are connected to each other~~, thereby to form a second input terminal; and

a source terminals of said P-type semiconductor element is connected to a source terminal of said ~~and~~ N-type semiconductor element ~~are connected to each other~~, thereby to form an output terminal.

Claim 19 (withdrawn)

Claim 20 (original): The semiconductor device of Claim 18, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

Claim 21 (withdrawn)

Claim 22 (Currently Amended): The semiconductor device of Claim 1, wherein:

[each of said semiconductor elements is composed of a P-type semiconductor element and an N-type semiconductor element;]

a high potential is supplied to a drain terminal of said N-type semiconductor element and a low potential is supplied to a drain terminal of said P-type semiconductor element;

a gate terminal of said N-type semiconductor element is connected to ~~and~~ a substrate terminal of said P-type semiconductor element ~~are connected to each other~~, thereby to form the first input terminal;

a gate terminal of said P-type semiconductor element is connected to ~~and~~ a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form the second input terminal; and

a source terminals of said P-type semiconductor element is connected to a source terminal of said ~~and~~ N-type semiconductor element ~~are connected to each other~~, thereby to form an output terminal.

Claim 23 (withdrawn)

Claim 24 (original): The semiconductor device of Claim 22, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said first input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said high potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

Claim 25 (withdrawn)

Claim 26 (original): The semiconductor device of Claim 18, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a

threshold voltage becomes higher than said low potential and lower than said high potential when said second input terminal is supplied with said low potential, and lower than said low potential when said second input terminal is supplied with said high potential.

Claim 27 (withdrawn)

Claim 28 (original): The semiconductor device of Claim 22, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said first input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said low potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said second input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said low potential.

Claims 29-36 (withdrawn)